OMC Project Description – DSP Image Processing System

High-speed image processing of target features is required in a number of applications in areas as diverse as motion analysis and embedded assembly. A DSP based system was created that enabled the processing of up to 100 targets in 20 milliseconds.

Overview

High speed image processing is required in many application areas. OMC developed a hybrid hardware and software solution for the sub-pixel location and tracking of small bright dots in an image that was otherwise relatively dark.

Industrial partners

Government and the Worshipful Company of Scientific Instrument Makers

Project duration

4 years

Project value

Approximately £ 70k

Intended beneficiaries

Manufacturing and Instrument Manufacturers

Current status

Technology used in Sewer Profiler, Licensed to a major instrument manufacturer.

Project Highlights

- DSP in Action Award Winner in 1998. Award sponsored by New Electronics, DSP 98 exhibition and Electronics Weekly

- Development and refinement of system for use in the development of a new product for a major instrument manufacturer

Background

DSP-90 is a series of stackable modules that can be used for a variety of purposes

- DSP-90 - Analog Devices 2101 Digital Signal Processor (DSP)
- VFE-90 - Video feature extractor
- GPIO-90 - General Purpose Input Output
- ENET-90 - Ethernet communications
- MOTOR/ENC-90 - 2 channel DC motor controller and 2 channel optical encoder
- PSU-90 - Wide band input power supply unit

DSP-90 has being used by:

- BAe Systems in a light stripe system and an optical triangulation system
- Thames Water in a sewer inspection system (Sewer RAT)
- City University in a real-time 3-D measurement system

Specification:

- Stackable 90 mm diameter modules
- 10/20 MHz Digital Signal Processor capable of executing single cycle multiply and accumulate operations in parallel with other operations such as memory fetches or barrel shifts.
- 4 x 8 bit I/O ports
- 2 x 16 bit FIFO inputs
- Communications via Ethernet, PC parallel or serial port
- 2 x DC motor controller outputs
- 2 x 5000 count per revolution incremental optical encoder inputs
- 9-18 Volt or 18-36 Volt input voltage at approximately 1 amp
- 1 x CCIR video camera input with real-time threshold operation
- Windows NT and 98 interfaces

Pictorial highlights

DSP-90 Digital signal processor module

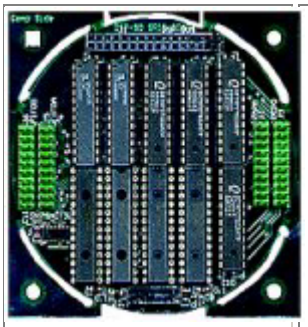
The DSP-90 module uses an Analog Devices ADSP2101 fixed point processor operating at 20 MHz. The ADSP2101 has both its' architecture and instruction set optimised for fast numerical processing. The processor has 16K words (16-bit) of data and 16K words (24-bit) of program memory, of which 2K words of data memory and 1K words of program memory are on-chip. 128 words of the external data memory space is used for memory-mapped I/O ports. The rest of the external data and program memory spaces are filled with 30nS SRAM. The 16K words (24-bit) of boot memory space is occupied by a 70nS EPROM. The processor divides this memory space into 2K words pages (0-7), page 0 contains 2-D processing and data communication software. Upon power up, the ADSP2101 loads a predefined page into the on-chip program memory. Software controlled rebooting is possible.

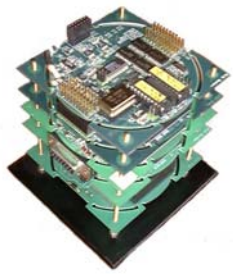
VFE-90 Video feature extractor

The video processor board is a mixed-mode circuit, comprising both analogue and digital circuitry. Analogue circuitry is concerned with video conditioning, whilst digital circuitry is utilised for hardware processing of the digitised video signal, and for interfacing with the DSP-90 system. A typical image of retro-reflective targets obtained under optimum lighting conditions will consist of a number of bright peaks in the image that are similar to the Point Spread Function of the lens. A single level threshold will be sufficient to encompass the majority of grey levels associated with each target for minimum error target location using the squared intensity centroid method which has been extensively tested. Under these circumstances the grey scale information necessary for each target amounts to around 25 pixels per target. Hence, for a 752x582 image containing 300 targets will only be using 25*300 / 438 k, i.e. less than 2% of the image.

The approach used in the VFE-90 module is to perform this operation in hardware. To achieve this one of the GPIO-90 ports is used to load a digital threshold level into a latch. The line-by-line video signal is A-D converted by a 10 bit Burr Brown converter and the output is compared with the threshold level. If this is the first edge encountered in the line the pixel location of this pixel is stored in a 16 bit word First In First Out (FIFO) buffer along with its intensity value. Any subsequent contiguous pixel intensity which is above the threshold is also stored. The same process is then repeated for all parts of the image that are above the threshold for that line. The next line is processed in the same manner. Prior to the beginning of each line a value of 0000 is stored in the FIFO denoting each line. In the case discussed the total storage required would be 582 + 300 * 25 FIFO = 8082 words. For interlaced imagery the odd-even field output of the synchronisation stripper is used to direct the data to one of two FIFOs one for odd lines and the other for the even lines. Each FIFO can be either 4 K or 8 K words. By performing the processing at the hardware level the data which requires processing is reduced considerably.

The VFE-90 board has been designed to be used with a variety of image formats. A voltage controlled crystal oscillator (VCXO) is used to enable high stability Phase Locked Loop synchronisation of CCIR or NTSC imagery. The pull in range for the VCXO is +/- 300 ppm. The pixel jitter

	for the circuit used is quoted as being less than 2 nsec. The counters are programmable via a GAL device and analogue imagery of up to 2k x 2k are possible. In addition there is a pixel clock input option as well as a line scan sensor option. The video processor board is built around a well specified video digitiser circuit. The ADC function is provided by a state of the art Burr-Brown 10 bit pipeline converter. This converter is driven by an amplifier configuration having a response up to 1 GHz. This specification allows settling times to 10 bit accuracy to be achieved in around 15 nsec. Considering a typical CCIR camera, with pixel clock running at around 14 MHz, the corresponding period for each pixel is around 75 nsec. Hence the amplifier network is able to settle to the converter accuracy prior to the conversion
 *GPIO-90 General purpose Input and Output module*	The GPIO-90 module provides two functions only. Input/output ports and FIFO ports. Four I/O ports are provided which can be read or write 8 bit data in latched or strobe mode. These ports can be used for a variety of purposes depending on how many are used for the main DSP-90 hardware. Options that currently exist are the operation of two DC Motors using a pulse-width-modulation (PWM) controller which is part of the PWM-ENC-90 card. Obvious uses with 3-D NET are pan and tilt mounts, synchronisation of flash lighting, and illumination of LED targets.
 *ENET-90 Ethernet communications module*	The Ethernet communications module uses the NE2000 chipset which is almost a de facto standard for 10 Mbits/second Ethernet. The module requires a packet driver in the same way that a PC does. The packet driver senses when data arrives and interrupts the DSP-90 processor so that the data can be collected. When a packet is required to be sent to an Ethernet address the DSP-90 sends the data to the ENET-90 board in the correct manner and initiates the sending process. Software has been written to communicate with Windows Sockets providing a hardware independent scheme for communication with the DSP system.
 *MOTOR/ENC-90 - DC motor controller and optical encoder input*	This module provides two Pulse Width Modulation controlled DC motor outputs. Small DC motors can be driven directly. The DSP-90 processor can change the speed of the motor by writing to a port. 10 speed levels can be set. In addition two optical encoder inputs are provided for up to 5000 step incremental encoders. The two quadrature inputs plus the home pulse input are used to count the current angular position of the encoder. This position is read via the FIFO ports into the DSP-90 processor.

 *PSU-90 Power supply unit module*	This module uses up to three DC-DC converters to allow a wide band input signal (9-18 Volts, or 18-36 Volts) to produce the voltage levels required. The inputs are protected from over and under voltage. CCD cameras, lasers, and motors can be driven from the same supply if necessary
	A stack of DSP modules
	A set of boxed DSP systems